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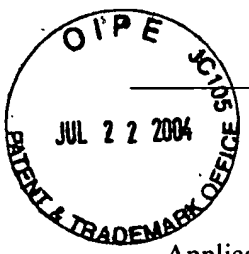

Case Docket No. IMEC329.001AUS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Catthoor et al.
Appl. No.	:	10/817,310
Filed	:	April 2, 2004
For	:	DESIGN METHOD FOR ESSENTIALLY DIGITAL SYSTEMS AND COMPONENTS THEREOF AND ESSENTIALLY DIGITAL SYSTEMS MADE IN ACCORDANCE WITH THE METHOD
Examiner	:	Unassigned
Group Art Unit	:	2825

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

7/20/2004
(Date)

E. M. Nelson
Eric M. Nelson, Reg. No. 43,829

TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application are:

(X) An Information Disclosure Statement.

(X) A PTO Form 1449 with twenty-one (21) references.

(X) The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.

(X) Return prepaid postcard.

E. M. Nelson

Eric M. Nelson
Registration No. 43,829
Attorney of Record
Customer No. 20,995
(619) 235-8550

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INFORMATION DISCLOSURE STATEMENT

Applicant	:	Catthoor et al.
App. No.	:	10/817,310
Filed	:	April 2, 2004
For	:	DESIGN METHOD FOR ESSENTIALLY DIGITAL SYSTEMS AND COMPONENTS THEREOF AND ESSENTIALLY DIGITAL SYSTEMS MADE IN ACCORDANCE WITH THE METHOD
Examiner	:	Unassigned
Group Art Unit	:	2825

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed is form PTO-1449 listing twenty-one references that are also enclosed.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required in accordance with 37 C.F.R. § 1.97(b)(3). If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 6/20/2004

By: _____

Eric M. Nelson
Registration No. 43,829
Attorney of Record
Customer No. 20,995
(619) 235-8550

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. IMEC329.001AUS	APPLICATION NO. 10/817,310
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	APPLICANT Catthoor et al.	
	FILING DATE April 2, 2004	GROUP 2825

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	1	B.Amrutur et al. "Speed and Power Scaling of SRAM's", IEEE Journal of Solid-state Circ., Vol. 35 No. 2, pp.175- 185, Feb. 2000.
	2	E.Brockmeyer et al. "Systematic Cycle budget versus System Power Trade-off: a New Perspective on System Exploration of Real-time Data-dominated Applications", Proc. IEEE Intnl. Symp. on Low Power Design, Rapallo, Italy, pp.137-142, Aug. 2000.
	3	J.A.Davis et al. "Interconnect limits on gigascale integration (GSI) in the 21st century", Proc. of the IEEE, No.3, Vol.89, pp.305-324, March 2001.
	4	R.Ho et al. "The future of wires", Proc. Of the IEEE, Vol.89, No.4, pp.490-504, April 2001.
	5	K.Itoh et al., "Limitations and challenges of multi-gigabit DRAM chip design", IEEE J. of Solid-state Circ., Vol. 32, No. 5, pp.624-634, May 1997.
	6	D.Sylvester et al., "Impact of small process geometries on microarchitectures in systems on a chip", Proc. of the IEEE, Vol.89, No.4, pp.467-489, April 2001.

EXAMINER	DATE CONSIDERED

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. IMEC329.001AUS	APPLICATION NO. 10/817,310
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT Catthoor et al.	
(USE SEVERAL SHEETS IF NECESSARY)	FILING DATE April 2, 2004	GROUP 2825

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	7	A. Vandecappelle et al., "Global Multimedia System Design Exploration using Accurate Memory Organization Feedback" Proc. 36th ACM/IEEE Design Automation Conf., New Orleans LA, pp.327-332, June 1999.
	8	S.J.E.Wilton et al., "CACTI: An enhanced cache access and cycle time model", IEEE J. of Solid State Circuits, Vol.31, No.5, pp.677-688, May 1996.
	9	S. Wuytack et al., "Minimizing the Required Memory Bandwidth in VLSI System Realizations", IEEE Trans. on VLSI Systems, Vol.7, No.4, pp.433-441, Dec. 1999.
	10	R. J. Evans et al., "*Energy Consumption Modeling and Optimization for SRAM's*, IEEE Journal of Solid-State Circuits, Vol.30, No.4, pp.571-579, May 1995.
	11	T. Seki et al., *A 6-ns 1-Mb CMOS SRAM with Latched Sense Amplifier*, IEEE Journal of Solid-State Circuits, Vol.28, No.4, pp. 478-483, April 1993.
	12	A. P. Chandrakasan et al., "*Low-Power CMOS Digital Design*", IEEE Journal of Solid-State Circuits, no.4, vol.27, pp. 473, April 1992.
	13	J. Lachman et al., "A 500MHz 1.5MB cache with on-chip CPU", Proceedings of the ISSC Conference (1999) p. 192.
	14	A. Chandrakasan et al., "A Low Power Chipset for Portable Multimedia Applications", (1994) IEEE International Solid-State Circuits Conf., pgs 82-83.
	15	A. Papanikolaou et al., "Interconnect Exploration for Future Wire Dominated Technologies" (2002)
	16	http://research.compaq.com/wrl/people/jouppi/Cacti.h, "Cacti", Accessed prior to April 4, 2003 and retrieved after April 2, 2004.
	17	Rambus, "Gigahertz Rambus Signaling Technologies" (2001) pgs. 1-4.
	18	http://www.research.compaq.com/wrl/projects/memorySystems/m, "Memory System Project", (2000) pgs 1-3.
	19	Sylvester et al., "Getting to the Bottom of Deep Submicron II: A Global Wiring Paradigm". (1999)
	20	Doug Matzke, "Will Physical Scalability Sabotage Performance Gains?", (1997), pgs 37-39.
	21	Arden et al., "International Technology Roadmap for Semiconductors" (2001)

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EXAMINER	DATE CONSIDERED
*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.	